InCore Semiconductors

Accelerating Custom Silicon

Observed Trends in Semiconductor Design

General-purpose CPUs are struggling to keep pace with ever-evolving workloads: Media, Virtualization, Automation, AI, VR, Comms/Signal processing.

Achieve higher efficiency by tailoring the architecture to the characteristics of the domain. This is done by effective use of memory bandwidth, leverage domain specific parallelism and avoid redundant compute.

Large time and cost spent in front-end SoC design exploration and stitching.

Legacy IP, Tooling and Methodologies are labour intensive and cannot scale as fast & efficiently as required to address the growing need for customization

This trend is now catching up in the **embedded segment** at a rapid pace:
Smart Homes, speakers, automotive, infotainment, etc.

How to build Custom SoCs - Fast & Better ?

- Fine Tuned Processors
- Optimized NoCs
- Rapid RTL Stitching
- Automated Verification
- Software and Docs

Underlying tech needs to inherently enable:

Configurability
Customizability
Extensibility

Configurable ISA
RISC-V®

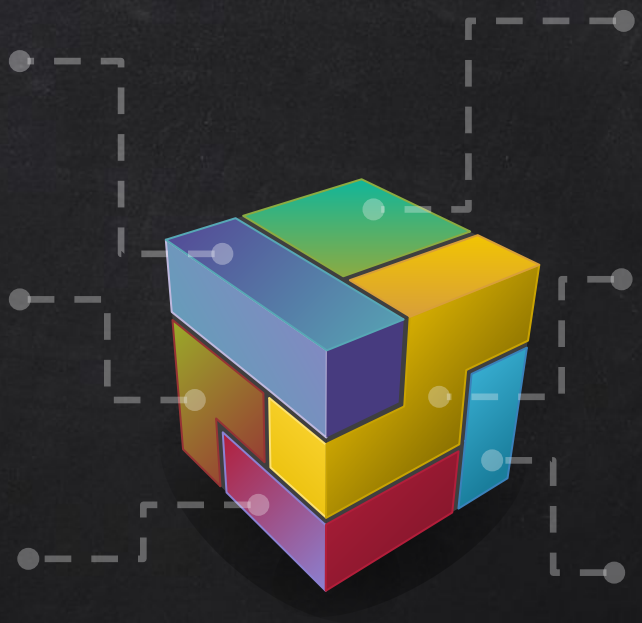
Generator Tech
BSV + Python + eUVM + ADOC
Exercise Automation by Default

Partnerships
Engage with IP partners for a robust ecosystem

Collapsing Time, Effort and Barrier to build Custom SoCs

The SoC SubSystem Generator

The Swiss Army Knife for all things Custom



YAML for SoC Specification

Reduces the ambiguity inherent in traditional. Capture configs for peripherals, cores, nocs, clock domains, interrupts, side-bands, verification, sdk,etc. Machine-readable and executable **improving readability and maintainability.**

RISC-V Core Generator

Each family of InCore Core Generators can be configured and customized at the ISA and the micro-architectural levels to provide a tailored RISC-V compatible core. **Matches equivalent ARM cores in PPA.**

Verification Generator

The generator is capable for creating verification environments and stimulus for various components like : **Directed and Random Assembly tests for the RISC-V Cores, Stress tests for the NoC, RDLs, RALs, UVM Models, etc.**

Python Based Automation

Defines a unique and **user-friendly API for plugin development and performs cross-category sanity checks** . Interfaces with popular EDA tools and development environments. Seamlessly works with various spec formats.

NoC Generator

A wide range of interconnect fabrics and components for embedded systems providing efficient and reliable communication. **Supports converters that adjust the clock and data signals between different IPs and modules.**

Software + Docs

Smart SDK Generator which includes customized **compiler toolchain for the specific SoC configuration and pre-configured build system and makefiles** . Also generates robust documents for end-users.

Biz Model & Target Segments

The SoC Subsystem Generator is currently an internal capability tool - Generating High Quality Custom IP

The IP revenue model is usually a mix of :
NRE, AMC and Royalty

The tool holds a **potential to be licensed as an EDA tool** in the future and thus enter enterprise sales as well.

Roadmap also includes verticalized SoC Generators for specific compute segments : **Automotive, Space, AI, etc.**

Target ICPs

(Merchant) Silicon Companies (NRE + AMC + Royalty)
Examples: NXP, Renesas, STMicro, etc.
Persona: Companies that build large number of Si products containing different set of cores and 3rd party IP

(Captive) Silicon Companies (NRE + AMC [+Royalty])
Examples: Rolls-Royce, Ola Krutrim etc.
Persona: Companies that require special (auto-grade, fault-tolerant, intelligent, etc) SoCs for in-house electronic system design.

Design Services Companies (NRE + Royalty)
Examples: HCL, Tessolve, TCS, Wipro, etc.
Persona: Companies that cater to a large number of end customers of Si-IP with varied market requirements.

Startups (Royalty)
Persona: New entrants in the market exploiting OEM/ODM opportunities for disruption.

The Team that can Deliver

InCore is a semicon design startup headquartered in **India (Chennai)**

Founded in 2018 by the creators of the **SHAKTI Processor Program at IIT-Madras** (started in 2012)

Providers of world class **RISC-V Solutions**
Founding member of RISC-V Foundation

Current strength: 30+
$3 Mn funding from PeakXV (formerly Sequoia Capital India), 2023

Founding Team: 100+ years of combined experience

G S Madhusudan
CEO
4 decades in SW & HW products

Neel Gala
CTO
PhD from IIT-Madras, Founder and Tech Lead for the Shakti Project.

Gautam Doshi
Chief Architect
3 decades of processor design at Intel

Arjun Menon
Chief Engineer
Masters from IIT Madras, Security expert

Milestones , Traction, etc...

1. Funding:
   a. Raised **USD 3Mn** from **PeakXV** (Sequoia Capital India) in March 2023
2. **Product Launches:**
   a. Azurite Core IPs were released in March ’24
   b. Calcite Core IPs were released in July ’24
3. We are **pre-revenue**
4. Traction milestones for 2024:
   a. **1 Core IP Design Win** , 4 IP evaluations
   b. 1 Enterprise pilot for SoC Subsystem Generator
   c. Government grants : **USD 1.1Mn**
   d. Deal pipeline for next 12 months (NRE) : **USD 1.2Mn**
5. Strategic **Partnerships** :
   a. HCL, Tessolve, Smart DV
6. **Team:**
   a. CPO, CMO hired
   b. Engg team expanded (8 ->28+)
   c. Second office in Bangalore

Competition

1. SiFive and Andes:
   a. Both are highly focused on delivering discrete RISC-V cores with minimal re-configuration
   b. Neither offers a configurable Soc Sub-System - which is key for RISC-V adoption.
2. Codasip:
   a. Offers a tool which can be used to build custom pipeline, however suffers from a learning curve
   b. Base templates are not competitive

ASKs

1. Support and guidance in Market access in USA and other key geographies
2. Biz dev support in the USA

THANKS

Contact info:

Neel (CTO) : neelgala@incoresemi.com